What is claimed is:

1. An interface for communicating between electronic components having multiple connection points, said interface comprising:

a circuit for a state machine to perform as a target and an initiator of a communication; and

a plurality of pins, connected to the circuit, said plurality of pins corresponding to a set of target signals handling communication involving the component as a target and a set of initiator signals handling communication involving the component as an initiator.

2. The interface of claim 1, wherein each of the plurality of pins are unidirectional and comprise at least one input pin and at least one output pin.

3. The interface of claim 2, wherein the number of input pins is equal to the number of output pins.

4. The interface of claim 3, wherein the set of target signals is symmetric with the set of initiator signals.

5. An electronic component comprising:

a circuit for a state machine to perform as a target and an initiator of a communication; and

a plurality of pins, connected to the circuit, said plurality of pins corresponding to a set of target signals handling communication involving the

component as a target and a set of initiator signals handling communication involving the component as an initiator.

6. The electronic component of claim 5, wherein each of the plurality of pins are unidirectional and comprise at least one input pin and at least one output pin.

7. The electronic component of claim 6, wherein the number of input pins is equal to the number of output pins.

8. The electronic component of claim 7, wherein the set of target signals is symmetric with the set of initiator signals.

9. An integrated circuit comprising:

(a) a bus;

(b) a plurality of functional blocks; and

(c) a plurality of ports, each port connecting the bus to one of the plurality of functional blocks;

wherein each of the plurality of ports is designed to perform as both a target and an initiator of a communication.

10. A computer-assisted model of an integrated circuit comprising:

(a) a bus model;

(b) a plurality of functional block models; and

(c) a plurality of port models, each port model connecting the bus model to one of the plurality of functional block models;

wherein each of the plurality of port models is designed to perform as both a target and an initiator of a communication.

11. A method of designing an integrated circuit comprising the steps of:

(a) specifying a communication block for the integrated circuit, including the locations of a plurality of androgynous interfaces;

(b) identifying the functional blocks to comprise the integrated circuit;

(c) positioning the blocks to form a layout of the integrated circuit to minimize connection distances between functional blocks and between functional blocks and the androgynous interfaces;

(d) setting the androgynous interfaces to perform as targets or initiators based on the layout.

12. The method of claim 11, wherein the communication block is part of a specified foundation block.